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IAP35
PATENT & TRADEMARK OFFICE

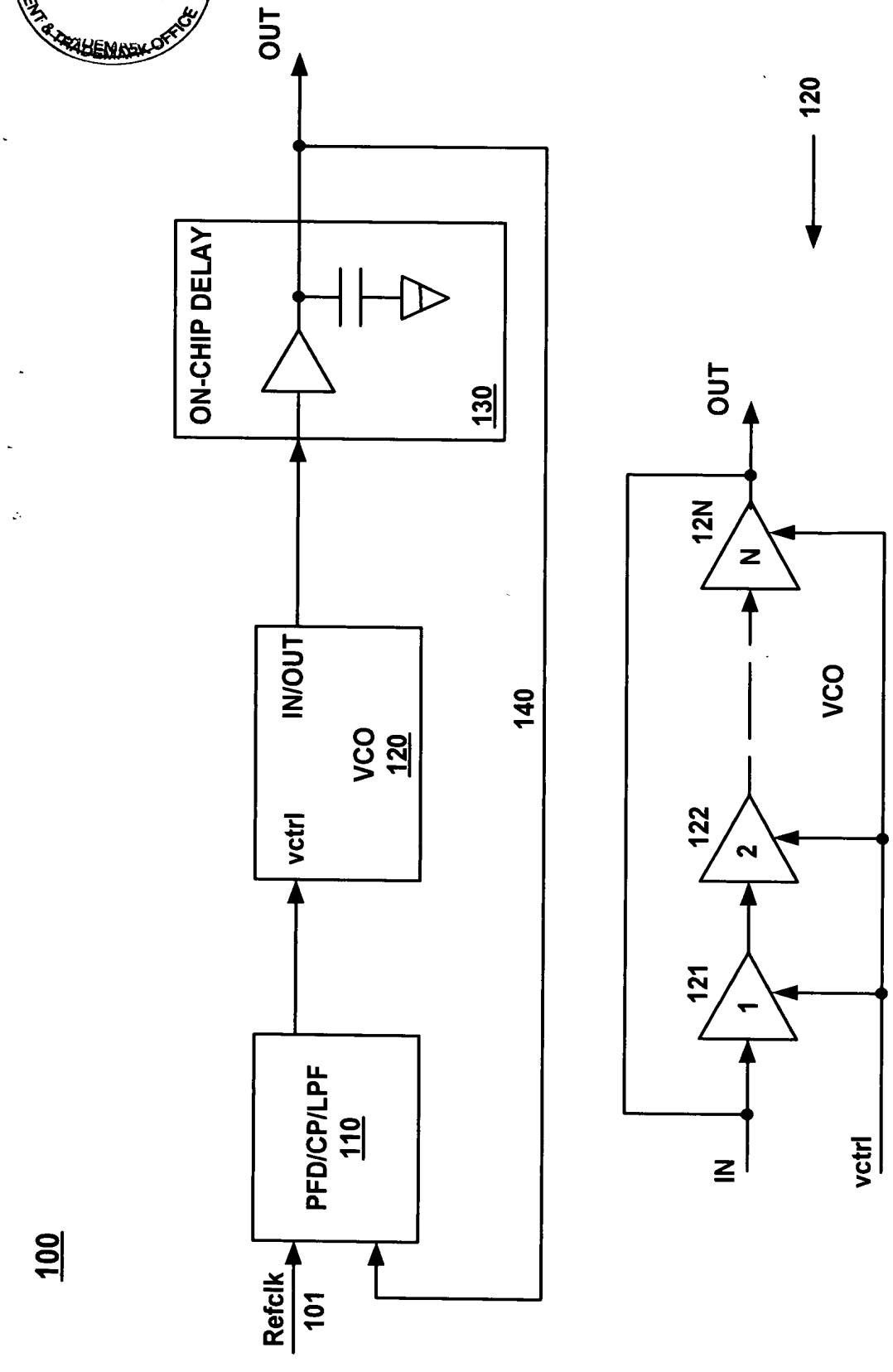

FIGURE 1
(PRIOR ART)

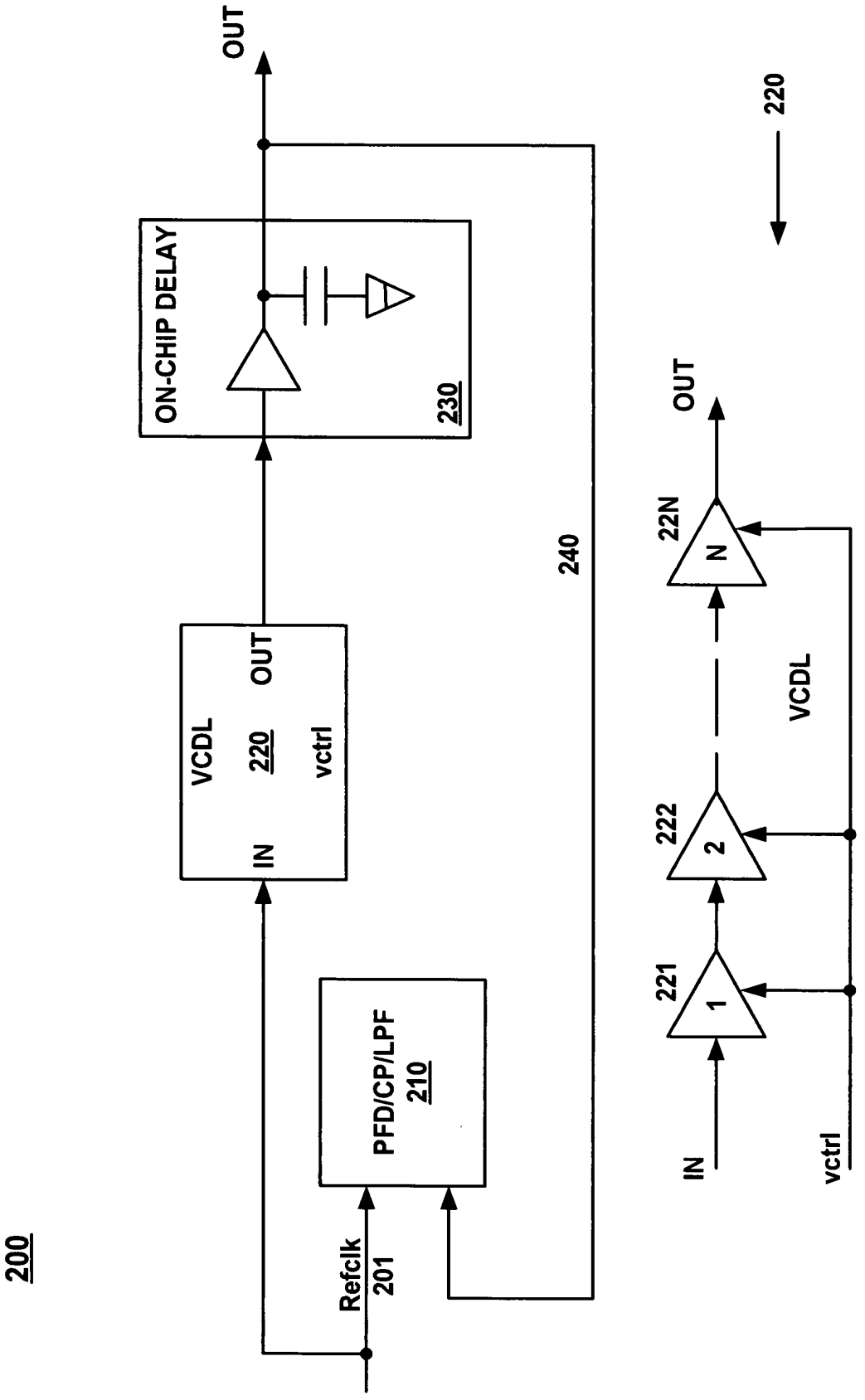

FIGURE 2
(PRIOR ART)

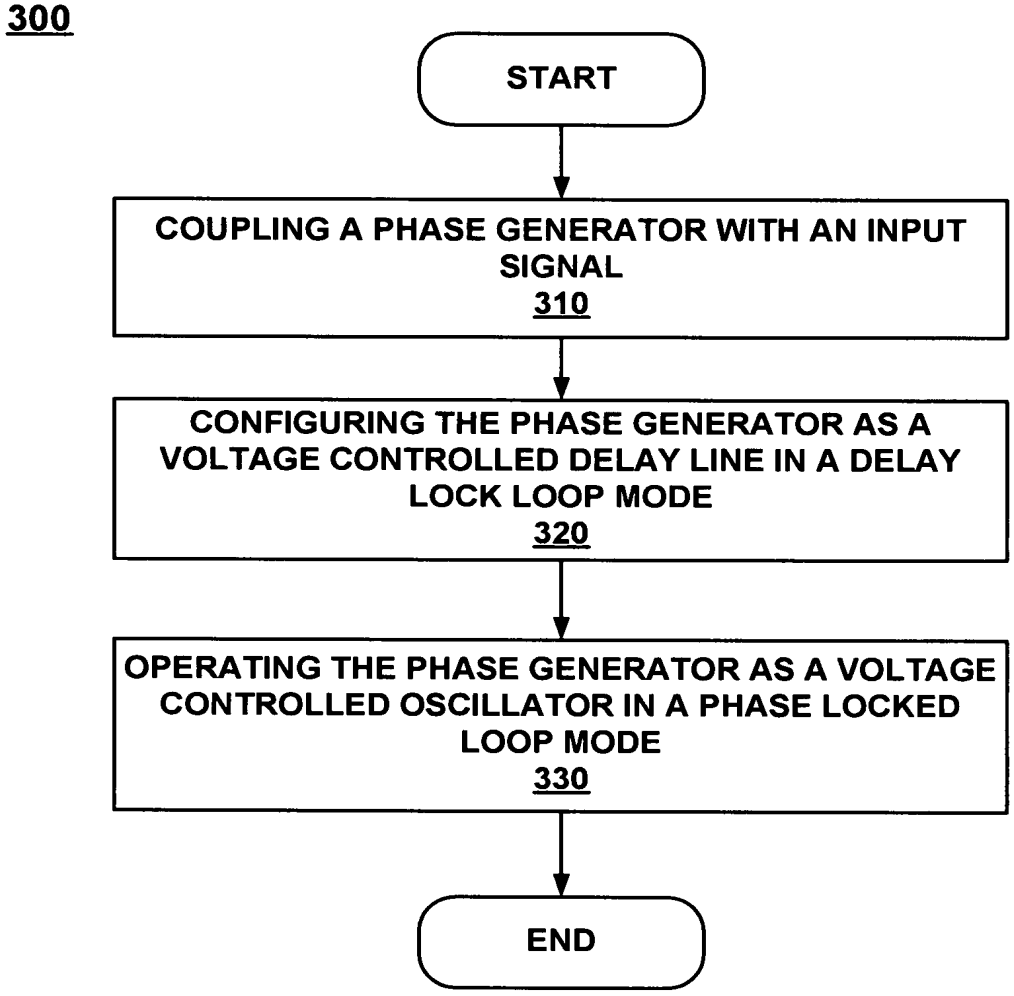
300
START
COUPLING A PHASE GENERATOR WITH AN INPUT SIGNAL
310
CONFIGURING THE PHASE GENERATOR AS A VOLTAGE CONTROLLED DELAY LINE IN A DELAY LOCK LOOP MODE
320
OPERATING THE PHASE GENERATOR AS A VOLTAGE CONTROLLED OSCILLATOR IN A PHASE LOCKED LOOP MODE
330
END

FIGURE 3

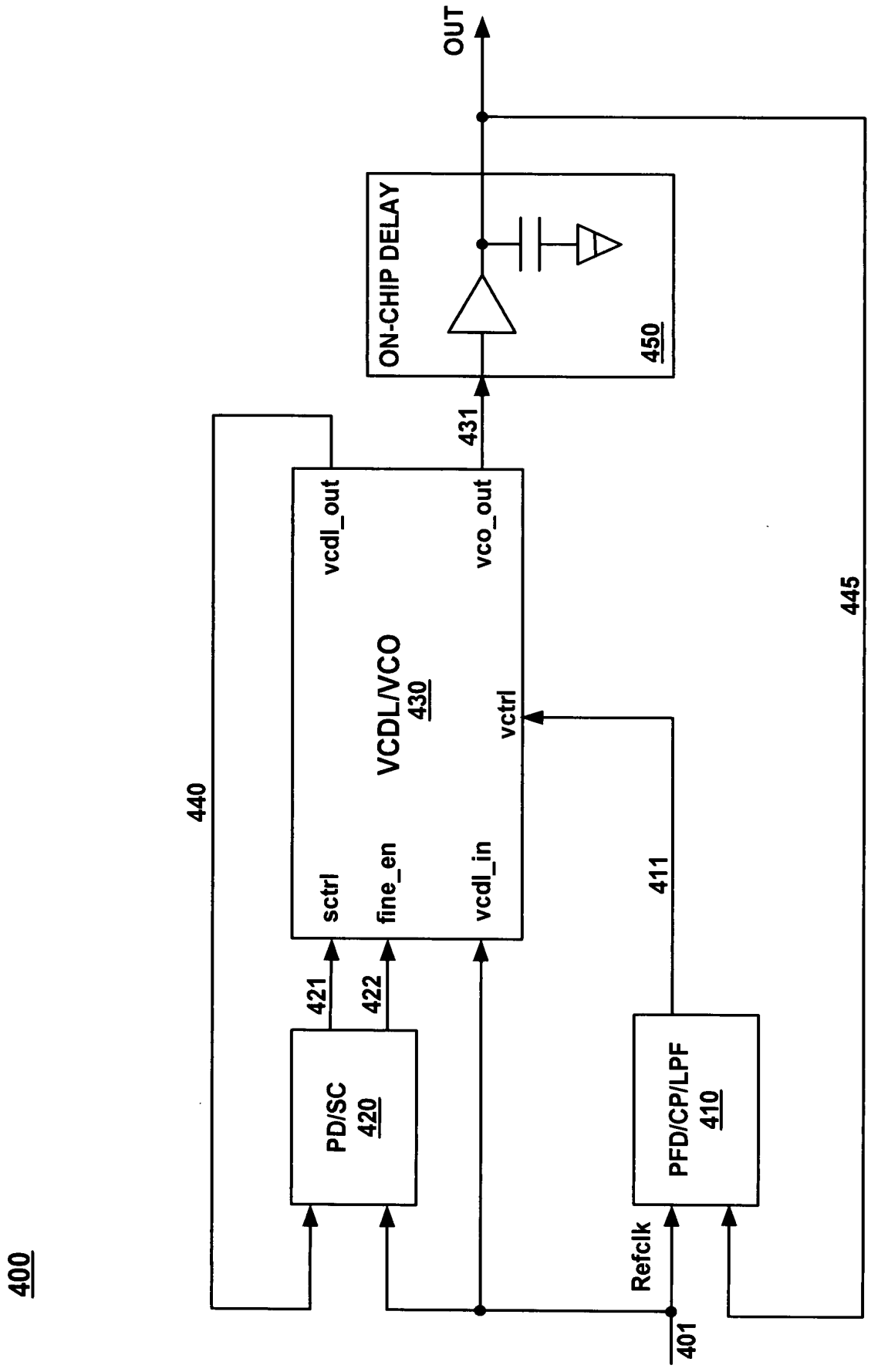
400
OUT
ON-CHIP DELAY
450
431
VCDL/VCO
430
vcdl_out
vco_out
vctrl
sctrl
fine_en
vcdl_in
440
445
411
421
422
PD/SC
420
PFD/CP/LPF
410
Refclk
401

FIGURE 4

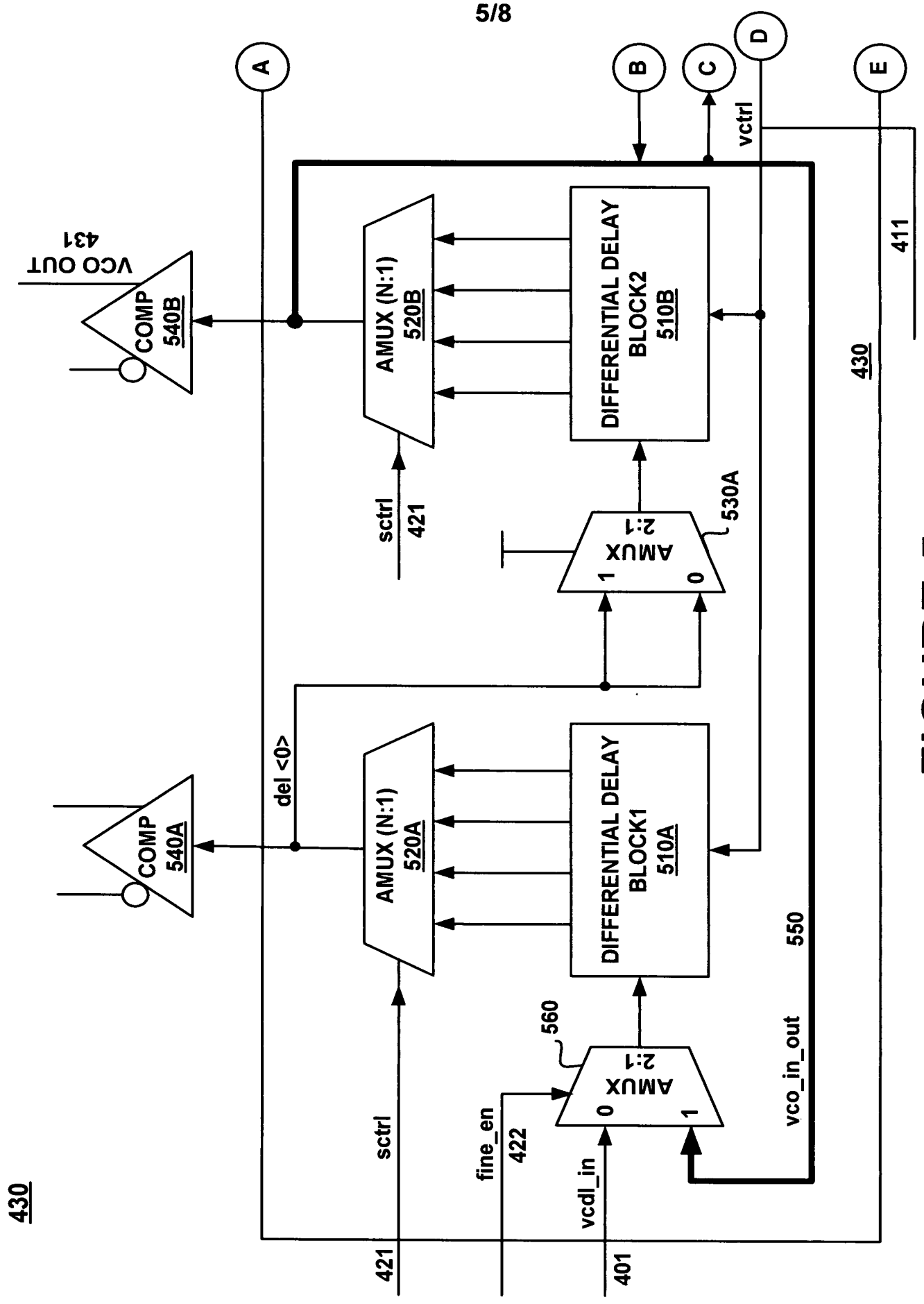
430
A
B
C
D
E
vctrl
411
430
VCO OUT
431
COMP
540B
AMUX (N:1)
520B
DIFFERENTIAL DELAY
BLOCK2
510B
sctrl
421
AMUX
2:1
530A
1
0
del <0>
COMP
540A
AMUX (N:1)
520A
DIFFERENTIAL DELAY
BLOCK1
510A
560
AMUX
2:1
0
1
sctrl
421
fine_en
422
vcdl_in
401
vco_in_out
550

FIGURE 5

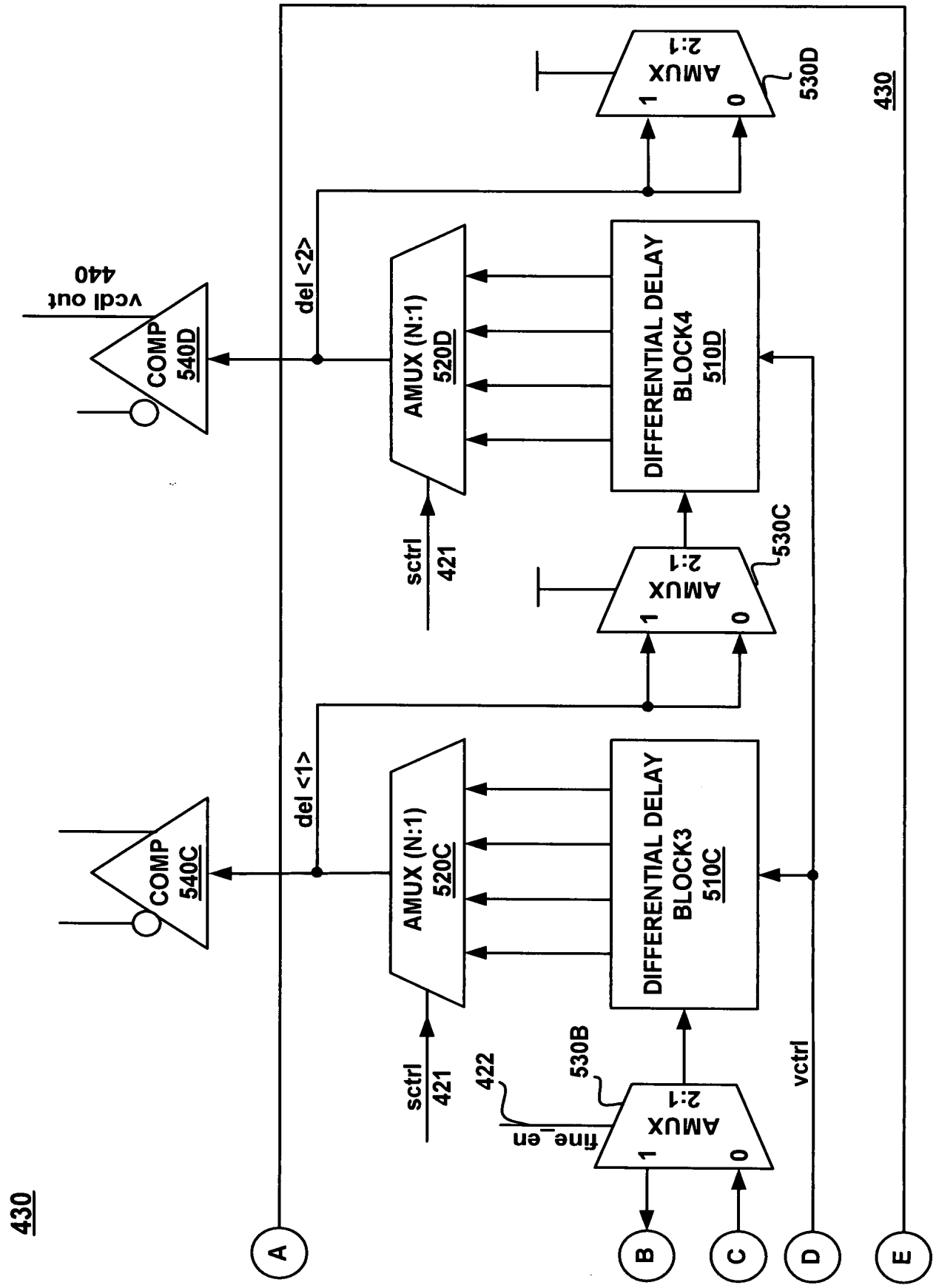

FIGURE 5 (CONT.)

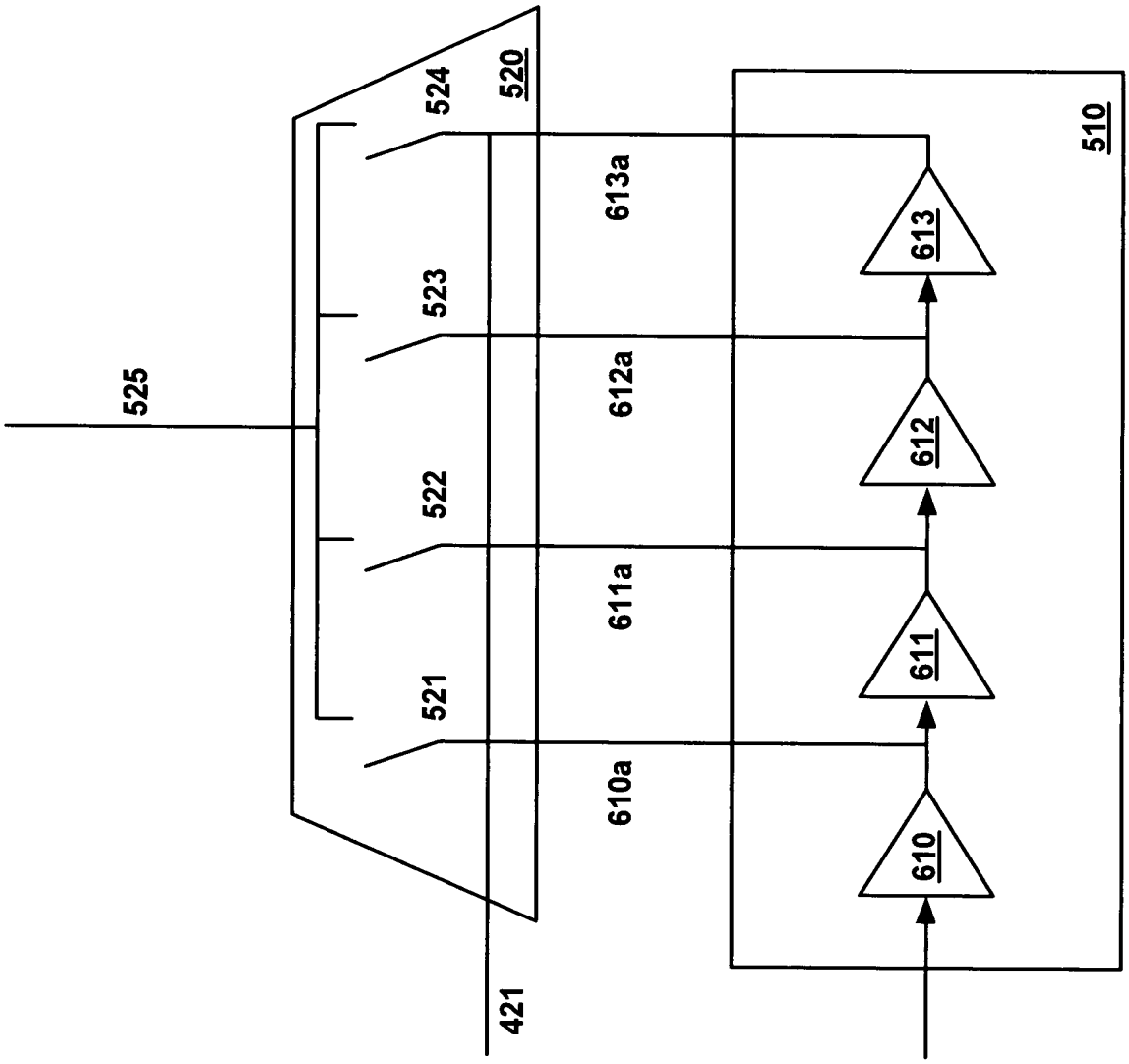
520
524
523
522
521
525
421
610a
611a
612a
613a
610
611
612
613
510

FIGURE 6

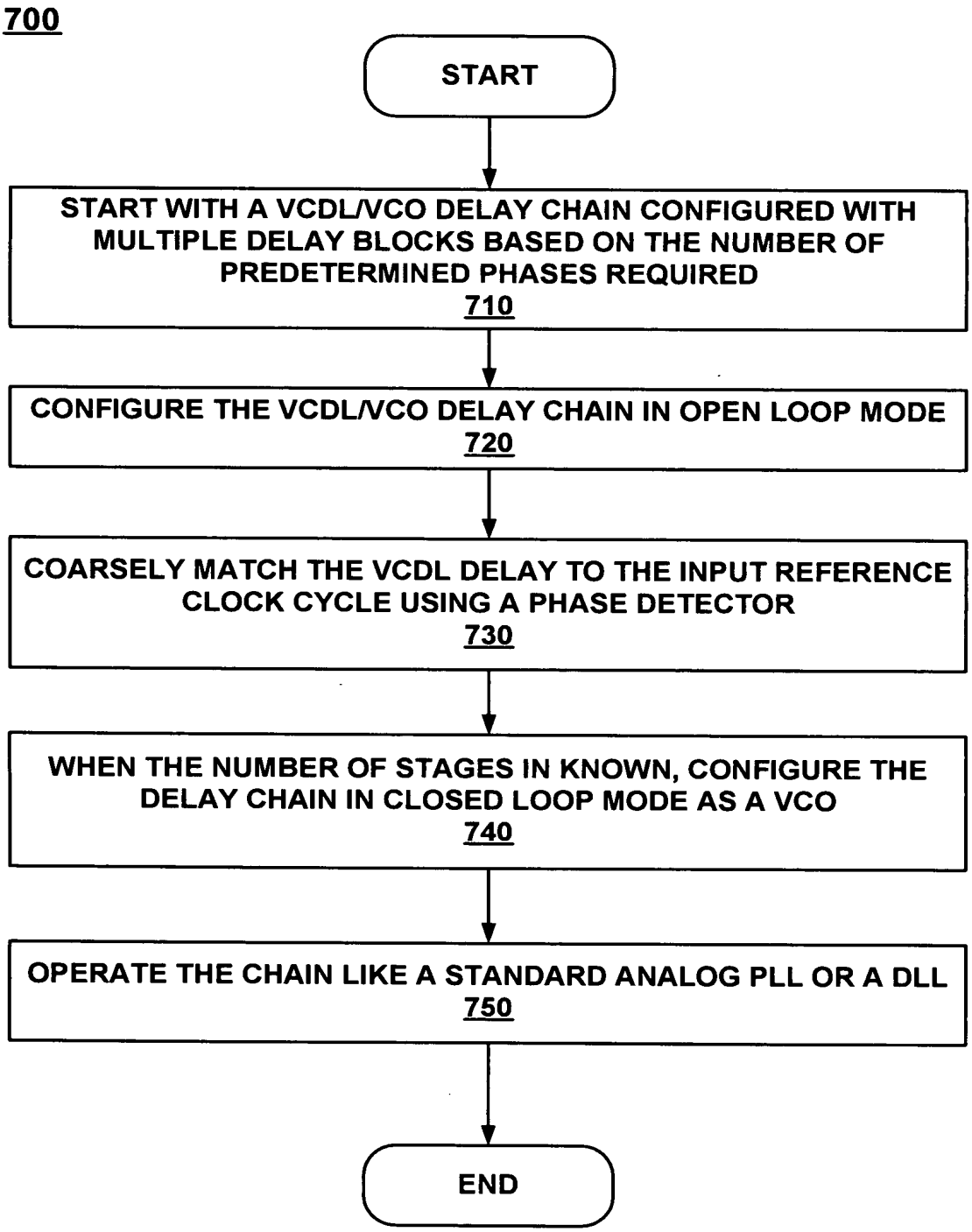
700
START
START WITH A VCDL/VCO DELAY CHAIN CONFIGURED WITH MULTIPLE DELAY BLOCKS BASED ON THE NUMBER OF PREDETERMINED PHASES REQUIRED
710
CONFIGURE THE VCDL/VCO DELAY CHAIN IN OPEN LOOP MODE
720
COARSELY MATCH THE VCDL DELAY TO THE INPUT REFERENCE CLOCK CYCLE USING A PHASE DETECTOR
730
WHEN THE NUMBER OF STAGES IN KNOWN, CONFIGURE THE DELAY CHAIN IN CLOSED LOOP MODE AS A VCO
740
OPERATE THE CHAIN LIKE A STANDARD ANALOG PLL OR A DLL
750
END

FIGURE 7